1. \_\_\_\_\_\_ are used to over come the difference in data transfer speeds of various devices.

A.)   https://www.indianstudyhub.com/images/write.png    Buffer registers

   **B.)**Bridge circuits

   **C.)**Multiple Buses

   **D.)**Multiple Buses

**Show Answer**

1. The main virtue for using single Bus structure is \_\_\_\_\_\_\_\_\_\_\_\_

   **A.)** Fast data transfers

   **B.)**Cost effective connectivity and speed

C.)   https://www.indianstudyhub.com/images/write.png    Cost effective connectivity and ease of attaching peripheral devices

   **D.)**None of these

1. To extend the connectivity of the processor bus we use \_\_\_\_\_\_\_\_

   **A.)** Controllers

   **B.)**Multiple bus

C.)   https://www.indianstudyhub.com/images/write.png    PCI bus

   **D.)**SCSI bus

1. IBM developed a bus standard for their line of computers ‘PC AT’ called \_\_\_\_\_

   **A.)** IB bus

B.)   https://www.indianstudyhub.com/images/write.png    ISA

   **C.)**M-bus

   **D.)**None of these

1. The bus used to connect the monitor to the CPU is \_\_\_\_\_\_

   **A.)** PCI bus

B.)   https://www.indianstudyhub.com/images/write.png    SCSI bus

   **C.)**Memory bus

   **D.)**Rambus

1. The ISA standard Buses are used to connect \_\_\_\_\_\_\_\_\_\_\_

   **A.)** RAM and processor

B.)   https://www.indianstudyhub.com/images/write.png    Harddisk and Processor

   **C.)**GPU and processor

   **D.)**CD/DVD drives and Processor

1. The main advantage of multiple bus organisation over single bus is \_\_\_\_\_

A.)   https://www.indianstudyhub.com/images/write.png    Reduction in the number of cycles for execution

   **B.)**Increase in size of the registers

   **C.)**Better Connectivity

   **D.)**None of these

1. During the execution of the instructions, a copy of the instructions is placed in the \_\_\_\_\_\_

A.)   https://www.indianstudyhub.com/images/write.png    Cache

   **B.)**Register

   **C.)**RAM

   **D.)**System heap

1. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_

   **A.)** Super-scaling

B.)   https://www.indianstudyhub.com/images/write.png    Pipe-lining

   **C.)**Parallel Computation

   **D.)**None of these

1. The clock rate of the processor can be improved by \_\_\_\_\_\_\_

   **A.)** Improving the IC technology of the logic circuits

   **B.)**Reducing the amount of processing done in one step

   **C.)**By using overclocking method

D.)   https://www.indianstudyhub.com/images/write.png    All of these

1. The ultimate goal of a compiler is to \_\_\_\_\_\_\_\_

   **A.)** Be able to detect even the smallest of errors

B.)   https://www.indianstudyhub.com/images/write.png    Reduce the clock cycles for a programming task

   **C.)**Reduce the size of the object code

   **D.)**Be versatile

1. As of 2000, the reference system to find the performance of a system is \_\_\_\_\_

   **A.)** Ultra SPARC 10

   **B.)**SUN SPARC

   **C.)**SUN II

   **D.)**None of these

1. The average number of steps taken to execute the set of instructions can be made to be less than one by following \_\_\_\_\_\_\_

   **A.)** ISA

B.)   https://www.indianstudyhub.com/images/write.png    Super-scaling

   **C.)**Pipe-lining

   **D.)**Sequential

1. If the instruction, Add R1, R2, R3 is executed in a system which is pipe-lined, then the value of S is (Where S is term of the Basic performance equation)

   **A.)** 3

   **B.)**~2

C.)   https://www.indianstudyhub.com/images/write.png    ~1

   **D.)**6

1. As of 2000, the reference system to find the SPEC rating are built with \_\_\_\_\_ Processor.

A.)   https://www.indianstudyhub.com/images/write.png    Ultra SPARC -IIi 300MHZ

   **B.)**Intel Atom SParc 300Mhz

   **C.)**Amd Neutrino series

   **D.)**ASUS A series 450 Mhz

1. CISC stands for \_\_\_\_\_\_\_

   **A.)** Complete Instruction Sequential Compilation

   **B.)**Computer Integrated Sequential Compiler

C.)   https://www.indianstudyhub.com/images/write.png    Complex Instruction Set Computer

   **D.)**Complex Instruction Sequential Compilation

1. When Performing a looping operation, the instruction gets stored in the \_\_\_\_\_\_

   **A.)** Cache

B.)   https://www.indianstudyhub.com/images/write.png    System Heap

   **C.)**System stack

   **D.)**Cache

1. SPEC stands for \_\_\_\_\_\_\_

   **A.)** Standard Performance Evaluation Code

   **B.)**System Processing Enhancing Code

C.)   https://www.indianstudyhub.com/images/write.png    System Performance Evaluation Corporation

   **D.)**Standard Processing Enhancement Corporation

.

1. An optimizing Compiler does \_\_\_\_\_\_

   **A.)** Better compilation of the given piece of code

B.)   https://www.indianstudyhub.com/images/write.png    Takes advantage of the type of processor and reduces its process time

   **C.)**Does better memory managament

   **D.)**none of the

.

1. The instruction -> Add LOCA, R0 does \_\_\_\_\_\_\_

   **A.)** Adds the value of LOCA to R0 and stores in the temp register

B.)   https://www.indianstudyhub.com/images/write.png    Adds the values of both LOCA and R0 and stores it in R0

   **C.)**Adds the value of LOCA with a value in accumulator and stores it in R0

   **D.)**Adds the value of R0 to the address of LOCA

1. During the execution of a program which gets initialized first ?

   **A.)** MAR

B.)   https://www.indianstudyhub.com/images/write.png    PC

   **C.)**MDR

   **D.)**IR

1. ISP stands for \_\_\_\_\_\_\_\_\_

A.)   https://www.indianstudyhub.com/images/write.png    Instruction Set Processor

   **B.)**Information Standard Processing

   **C.)**Interchange Standard Protocol

   **D.)**Interrupt Service Procedure

1. The decoded instruction is stored in \_\_\_\_\_\_

A.)   https://www.indianstudyhub.com/images/write.png    IR

   **B.)**PC

   **C.)**Registers

   **D.)**MDR

1. Which registers can interact with the secondary storage?

   **A.)** PC

   **B.)**R0

   **C.)**IR

D.)   https://www.indianstudyhub.com/images/write.png    MAR

1. Which of the register/s of the processor is/are connected to Memory Bus?

   **A.)** PC

B.)   https://www.indianstudyhub.com/images/write.png    MAR

   **C.)**IR

   **D.)**Both PC and MAR

1. The internal Components of the processor are connected by \_\_\_\_\_\_\_

   **A.)** Rambus

B.)   https://www.indianstudyhub.com/images/write.png    Processor bus

   **C.)**Processor intra-connectivity circuitry

   **D.)**Memory bus

1. The registers,ALU and the interconnection between them are collectively called as \_\_\_\_\_

   **A.)** information path

B.)   https://www.indianstudyhub.com/images/write.png    data path

   **C.)**process route

   **D.)**information trail

1. How many major companies around the world manufacture microprocessors?

**A** Only one company

**B** Tow companies

**C** Three companies

**D** Many companies

[View Answer](https://www.gkseries.com/mcq-on-computer-history/multiple-choice-questions-and-answers-on-computer-history#first)

Answer: Tow companies (Intel and Motorola)

1. **3** Which is an example of first generation computer?

**A** EDVAC

**B** EDSAC

**C** ENIAC

**D** UNIVAC

[View Answer](https://www.gkseries.com/mcq-on-computer-history/multiple-choice-questions-and-answers-on-computer-history#third)

Answer: ENIAC

1. **4** Operating system is used in which generation of computer for the first time?

**A** First Generation

**B** Second Generation

**C** Third Generation

**D** Fourth Generation

[View Answer](https://www.gkseries.com/mcq-on-computer-history/multiple-choice-questions-and-answers-on-computer-history#four)

Answer: Third Generation